Abstract

An interface for receiving data from an image sensor having an imaging array and a clock generator and for transferring the data to a processor system is described. The interface comprises a memory for storing the imaging array data and the clocking signals at a rate determined by the clocking signals. In response to the quantity of data in the memory, a signal generator generates a signal for transmission to the processor system and a circuit controls the transfer of the data from the memory at a rate determined by the processor system. The memory may be a first-in first-out (FIFO) buffer or an addressable memory. The interface is preferably integrated on the same die as the image sensor. The signal generator may generate either an interrupt signal for transmission to the processor system or a bus request signal for transmission to a bus arbitration unit for the processor system.